100Gbps QSFP28 LR4 Transceiver 10Km Reach

NM-7D9-LR4

1. Applications

- IEEE 802.3ba
- 100GBASE LR4

2. Features

- 4 channels full-duplex transceiver modules
- Transmission data rate up to 26Gbps per channel
- 4X26Gb/s DFB-based LAN-WDM Cooling transmitter
- 4 channels PIN ROSA
- Internal CDR circuits on both receiver and transmitter channels
- Support CDR bypass
- Low power consumption <3.5W
- Hot Pluggable QSFP form factor
- Up to reach 10Km for G.652 SMF
- Duplex LC receptacle
- Built-in digital diagnostic functions
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant(lead free)

Shenzhen NEM Engine Technology Co., Ltd.

Tel: 0086-400-966-4008 Fax: 0086-0755-86152561

E-mail:info@nemengine.com Web: www.nemengine.com

3. Description

NEM Engine's NM-7D9-LR4 is a 100Gb/s transceiver module designed for optical communication applications compliant to 100GBASE-LR4 of the IEEE P802.3ba standard. The module converts 4 input channels of 25Gb/s electrical data to 4 channels of LAN WDM optical signals and then multiplexes them into a single channel for 100Gb/s optical transmission. Reversely on the receiver side, the module de-multiplexes a 100Gb/s optical input into 4 channels of LAN WDM optical signals and then converts them to 4 output channels of electrical data.

The central wavelengths of the 4 LAN WDM channels are 1295.56, 1300.05, 1304.58 and 1309.14 nm as members of the LAN WDM wavelength grid defined in IEEE 802.3ba. The high performance cooled LAN WDM

DFB transmitters and high sensitivity PIN receivers provide superior performance for 100Gigabit Ethernet applications up to 10km links and compliant to optical interface with IEEE802.3ba Clause 88 100GBASE-LR4 requirements.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

4. standard

- Compliant with SFF-8636
- Compliant with IEEE 802.3bm
- Compliant with IEEE 802.3bj
- Ethernet 100GBASE-LR4
- RoHS compliance

5. Performance Specifications

5.1. Absolute Maximum Ratings

These values represent the damage threshold of the module. Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions.

Table.1 Absolute maximum ratings

Parameter	Symbol	Min	Max	Units
Supply voltage	Vcc	-0.3	3.6	V
Input Voltag	Vin	-0.3	Vcc+0.3	V
Storage temperature	Tst	-20	85	℃
Case Operating Temperature	Top	0	70	℃
Humidity(non-condensing)	Rh	5	85	%
Damage Threshold,each lane	TH	5.5		dBm

5.2. Recommended Operating Conditions

Table.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Units
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	℃
Data rate per lane	fd		25.78125		Gbps
Humidity	Rh	5		85	%
Power Consumption	P	-		3.5	W
Link Distance with G.652	D	0.002		10	Km

5.3. Transmitter Optical Characteristic

Table.3 Transmitter Optical Characteristic

Parameter	Symbol	Min.	Typical	Max.	Units	
Center Wavelength	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
SMSR	SMSR	30			dB	
Total Average Launch Power	Pt			10.5	dBm	
Average Launch Power,each Lane	PAVG	-4.3		4.5	dBm	
OMA,each Lane	POMA	-1.3		4.5	dBm	1
Difference in Launch Power	Ptx,diff			5	dB	
Launch power in OMA		-2.3			dBm	
TDP,each Lane	TDP			2.2	dB	
Extinction Ratio	ER	4			dB	
RIN20OMA	RIN			-130	dB/H	
Optical Return Loss	TOL			20	dB	
Transmitter Reflectance	RT			-12	dB	
Eye mask coordinates: X1,X2,X3,Y1,Y2,Y3		(0.25,0.4,0.45,0.25,0.28,0.4)				2
Average Launch Power OFF	Poff			-30	dBm	

5.4. Receiver Optical Characteristic

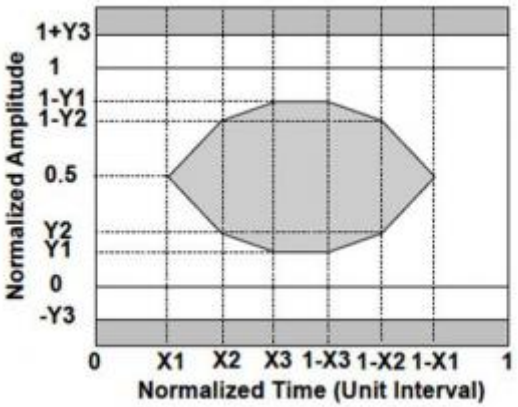
Table.4 Receiver Optical Characteristic

Parameter	Symbol	Min	Typ	Max.	Units	Conditions
Damage Threshold,each Lane	THd	5.5			dBm	3
Total Average Receive				10.5	dBm	
Average Receive Power,each Lane		-10.6		4.5	dBm	
Receive Power(OMA),each Lane				4.5	dBm	

Receiver Sensitivity(OMA),each Lane	SEN			-8.6	dBm	
Stressed Receiver Sensitivity(OMA),each Lane				-6.8	dBm	4
Difference in Receive Power between any Two Lanes(OMA)	Prx,diff			5.5	dB	
LOS Assert	LOSA	-18			dBm	
LOS Deassert	LOSD			-15	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency,each Lane	Fc			31	GHZ	
Vertical Eye Closure Pentalty, each Lane			1.8		dB	5
Stressed Eye J2 Jitter, Each Lane			0.3		UI	
Stressed Eye J9 Jitter, Each Lane			0.47		UI	

Note:

1. Even if the TDP < 1 dB, the OMA min must exceed the minimum value specified here.
2. See Figure 4 below.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Measured with conformance test signal at receiver input for BER = $1x10^{-12}$.
5. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



5.5. Electrical Specification

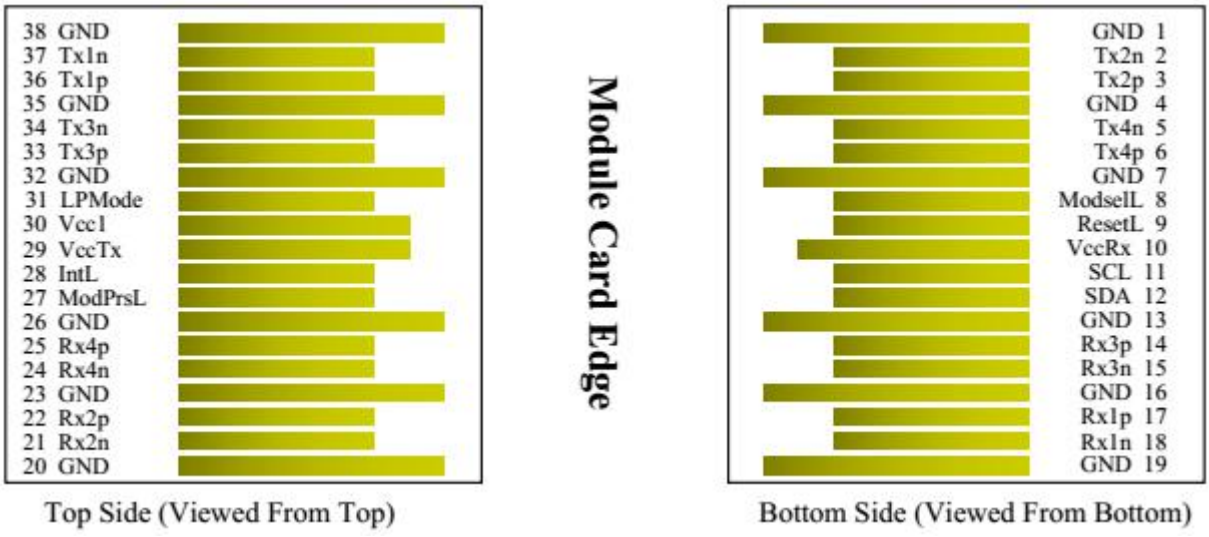
Table.5 Electrical Specification

Parameter	Symbol	Min	Typ	Max.	Units	Conditions
Power Consumption	P			3.5	W	
Supply Current	Icc			1.06	A	
Transceiver Power-on Initialization Time				2000	ms	
Transmitter(each Lane)						
Single-ended Input Voltage Tolerance		-0.3		4.0	V	
AC Common Mode Input Voltage Tolerance		15			mV	
Differential Input Voltage		50			mVpp	
Differential Input Voltage Swing	Vin			900	mVpp	
Differential Input Impedance	Zin	90	100	110	Ohm	
Receiver(each lane)						
Single-ended Output Voltage		-0.3		4.0	V	
AC Common Mode Output Voltage				7.5	mV	
Differential Output Voltage Swing	Vout	300		850	mVpp	
Differential Output Impedance	Zout	90	100	110	Ohm	

Note:

Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the modules is fully functional.b

5.6. Pin Definitions



Top Side (Viewed From Top)

Bottom Side (Viewed From Bottom)

She
Tel:
E-m

Table.6 Pin Definitions

Pin number	Logic	Symbol	Signal	Description
1		GND	Signal Ground	Ground
2	CML-I	Tx2n	Tx2n	Transmitter Inverted Date Input.AC coupled
3	CML-I	Tx2p	Tx2p	Transmitter Non_Inverted Date Input.AC coupled
4		GND	Signal Ground	Ground
5	CML-I	Tx4n	Tx4n	Transmitter Inverted Date Input.AC coupled
6	CML-I	Tx4p	Tx4p	Transmitter Non_Inverted Date Input.AC coupled
7		GND	Signal Ground	Ground
8	LVTTL-I	ModSelL	ModSelL	Module Select pin.Selected when held low by the host.
9	LVTTL-I	ResetL	LPMode_Reset	Module Reset.A"low" pulse induces a reset on the module.
10		Vcc Rx	Vcc Rx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	SCL	2-wire serial interface
12	LVCMOS-I/O	SDA	SDA	
13		GND	Signal Ground	Ground
14	CML-O	Rx3p	Rx3p	Receiver Non_Inverted Date Input.AC coupled
15	CML-O	Rx3n	Rx3n	Receiver Inverted Date Input.AC coupled
16		GND	Signal Ground	Ground
17	CML-O	Rx1p	Rx1p	Receiver Non_Inverted Date Input.AC coupled
18	CML-O	Rx1n	Rx1n	Receiver Inverted Date Input.AC coupled
19		GND	Signal Ground	Ground
20		GND	Signal Ground	Ground
21	CML-O	Rx2n	Rx2n	Receiver Inverted Date Input.AC coupled
22	CML-O	Rx2p	Rx2p	Receiver Non_Inverted Date Input.AC coupled
23		GND	Signal Ground	Ground
24	CML-O	Rx4n	Rx4n	Receiver Inverted Date Input.AC coupled
25	CML-O	Rx4p	Rx4p	Receiver Non_Inverted Date Input.AC coupled
26		GND	Signal Ground	Ground
27	LVTTL-O	ModPrsL	ModPrsL	Module Present pin.Internally grounded inside the module.
28	LVTTL-O	IntL	IntL	Interrupt by the QSFP module."Low"indicates an Alarm/Warning.
29		Vcc Tx	Vcc Tx	+3.3V Power Supply Transmitter
30		Vccl	Vccl	+3.3V Power Supply
31	LVTTL-I	LPMode	LPMode	Low Power Mode
32		GND	Signal Ground	Ground
33	CML-I	Tx3p	Tx3p	Transmitter Non_Inverted Date Input.AC coupled
34	CML-I	Tx3n	Tx3n	Transmitter Inverted Date Input.AC coupled
35		GND	Signal Ground	Ground
36	CML-I	Tx1p	Tx1p	Transmitter Non_Inverted Date Input.AC coupled
37	CML-I	Tx1n	Tx1n	Transmitter Inverted Date Input.AC coupled
38		GND	Signal Ground	Ground
Housing			Chassis Ground	

5.7. Power supply filtering

The host board should use the power supply filtering shown in Figure 1

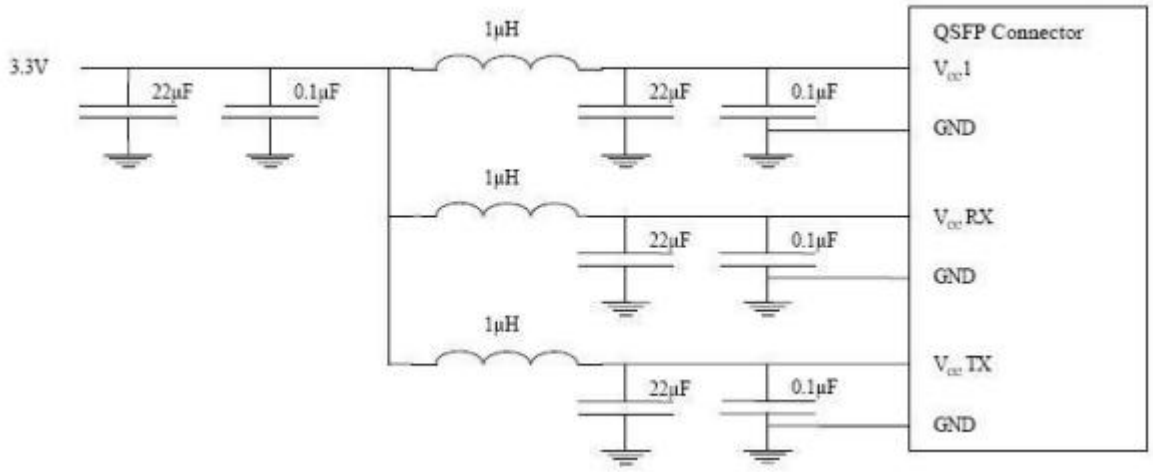


Figure 1:Host Board Power Supply Filtering

5.8. Functional Block Diagram of the QSFP Module

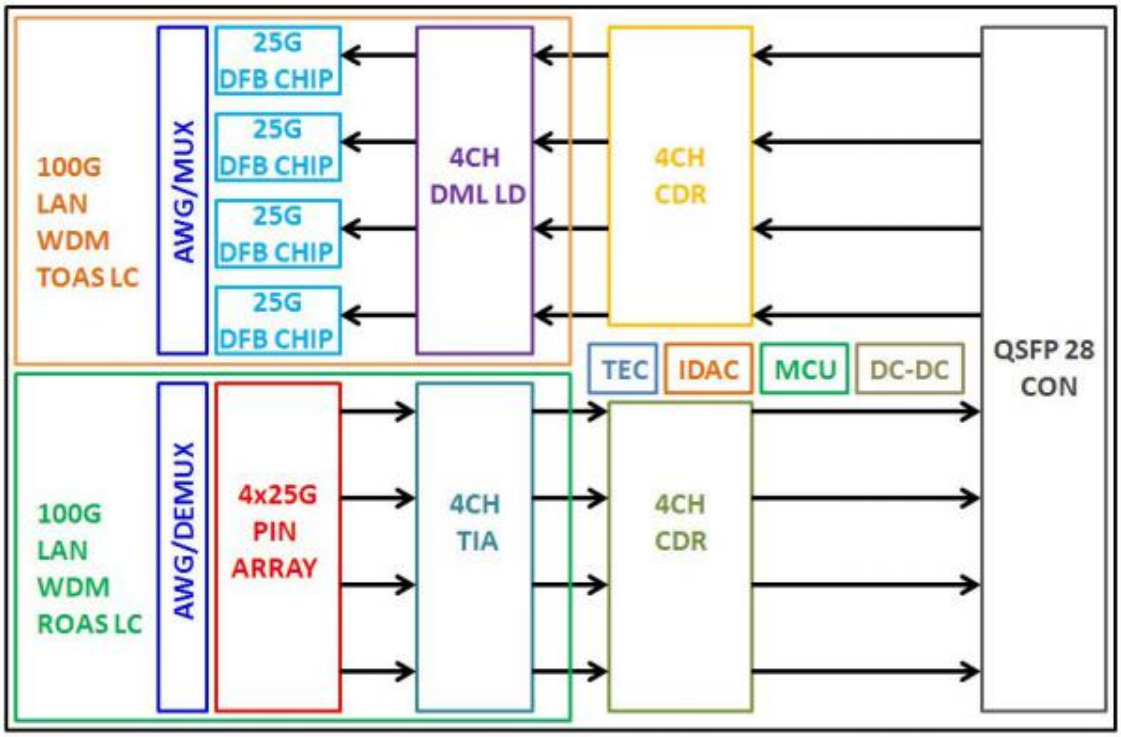


Figure 2:Module Block Diagram

5.9. Mechanical Dimensions

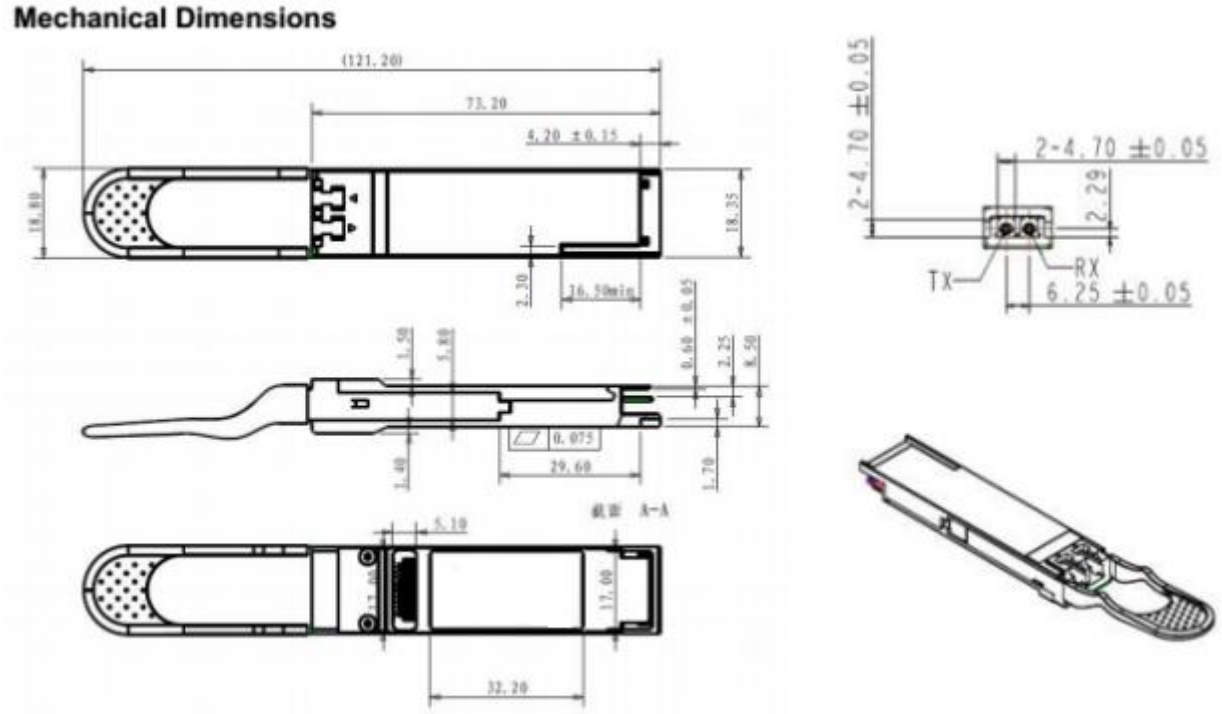


Figure 3:Mechanical Specifications

6. Aplication Cautions

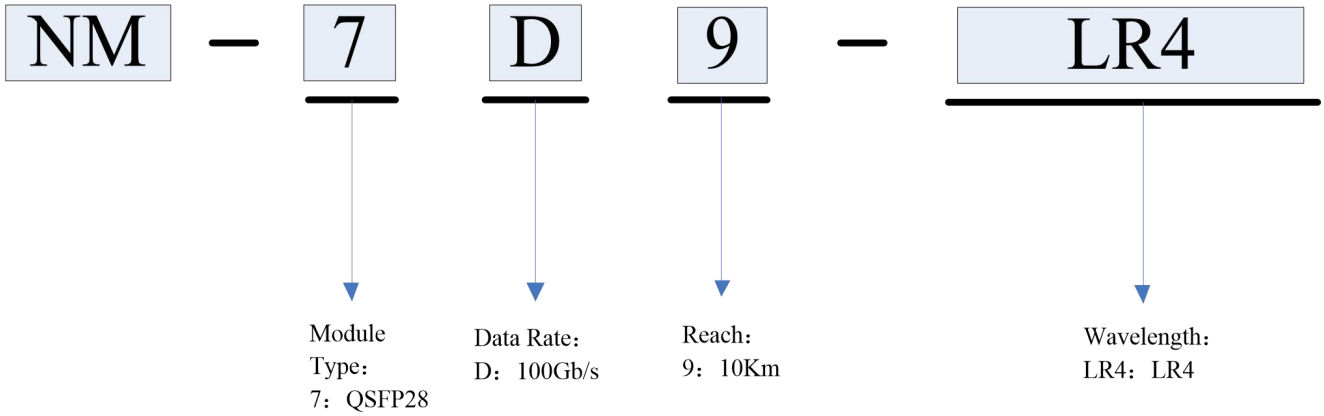
6.1. ESD

This transceiver is specified as ESD threshold 1kV for high speed pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

6.2. LASER SAFTY

This is a Class 1 Laser Product according to IEC 60825-1:1993:+A1:1997+A2:2001. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (July 26, 2001)

7. Order Information



Further Information

For further information, please contact NEME.

Tel: 0086-400-966-4008

Fax: 0086-0755-86152561

Web: www.nemengine.com

Add: 3/F, 20th Bldg. Guangqian Ind Zone. No.3 Longzhu Rd. Nanshan Dist. S.Z City, CHINA.