

100Gbps QSFP28 SR4 Transceiver 100m Reach

NM-7D0-SR4

1. Applications

- 100GBASE-SR4 Ethernet
- Datacom/Telecom switch&router connections
- Data Aggregation and backplane Applications
- Infiniband transmission at 4ch QDR,FDR and EDR



2. Features

- 4 channels full-duplex transceiver modules
- Transmission data rate up to 25Gbps per channel
- Support 40GE and 56G FDR data rate
- 4 channels 850nm VCSEL array
- 4 channels PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Support CDR bypass
- Low power consumption <2.5W
- Hot Pluggable QSFP form factor
- Maximum link length of 70m on OM3 Multimode Fiber (MMF)and 100m on OM4 MMF
- Single MPO connector receptacle
- Built-in digital diagnostic functions
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant(lead free)

Shenzhen NEM Engine Technology Co., Ltd.

Tel: 0086-400-966-4008

Fax: 0086-0755-86152561

E-mail:info@nemengine.com

Web: www.nemengine.com

3. Description

NEM Engine's NM-7D0-SR4 is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP+ SR4 for 100 or 40 Gigabit Ethernet, Infiniband FDR/EDR Applications. This transceiver is a high performance module for short-range multi-lane data communication and interconnect applications. It integrates four data lanes in each direction with 100 Gbps bandwidth. Each lane can operate at 25Gbps up to 70 m using OM3 fiber or 100 m using OM4 fiber. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 38 contact edge type connector. The optical interface uses an 12 fiber MTP (MPO) connector. This module incorporates Gigalight Technologies proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

A serial EEPROM in the transceiver allows the user to access transceiver monitoring and configuration data via the 2-wire QSFP Management Interface. This interface uses a single address, A0h, with a memory map divided into a lower and upper area. Basic digital diagnostic (DD) data is held in the lower area while specific data is held in a series of tables in the high memory area.

4. standard

- Compliant with SFF-8636 Rev 2.7
- Compliant with IEEE 802.3bm
- Compliant with IEEE 802.3bj
- Compliant with QSFP+ MSA
- GR-468-CORE
- RoHS compliance

5. Performance Specifications

5.1. Absolute Maximum Ratings

These values represent the damage threshold of the module. Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions.

Table.1 Absolute maximum ratings

Parameter	Conditions	Min	Max	Units
Power supply voltage at 3.3V		-0.3	4.5	V
Voltage on I/O pads		-0.3	VDD+0.3	V
Storage temperature	Non-condensing	-40	85	Celsius
Powered case temperature range	Non-condensing	-5	70	Celsius
Relative Humidity		5	95	%
Static discharge voltage on high speed pins	Human body model		500	V
Static discharge voltage on other pins	Human body model		2000	V
Air discharge to QSFP case	EN61000-4-2 Criterion B Test		15	kV
Contact discharge to QSFP case	EN61000-4-2 Criterion B Test		8	kV

5.2. Recommended Operating Conditions

Table.2 Recommended Operating Conditions

Parameter	Conditions	Min	Typ.	Max	Units
Data rate per lane	8B/10B Coding, 64B/66B Coding		25.78		Gbps
3.3V Supply Voltage		3.13	3.3	3.47	V
Power supply noise including ripples	1kHz to frequency of operation measured at VCC_HOST			50	mVpp
Case temperature		0	35	70	Celsius
Power Consumption	-	-	2	2.5	W
Supply Current	-	-		900	mA
Transmission Distance	om3			70	m
	om4			100	m

5.3. Transmitter Optical Characteristic

Table.3 Transmitter Optical Characteristic

Parameter	Symbol	Min.	Typical	Max.	Units
Center Wavelength	λ_C	840	850	860	nm
RMS Spectral width	$\Delta\lambda$			0.6	nm
Optical Power for TX DISABLE				-30	dBm
Average launch power, each lane	P	-8.4		2.4	dBm
Optical Modulation Amplitude (OMA), each lane	OMA	-6.4		3	
Launch power in OMA minus TDEC		-7.3			
Extinction Ratio	ER	3			
Signaling rate, each lane			25.78		Gbps
Optical eye mask		Compliant with IEEE std 802.3bm-2015			
Optical Return Loss Tolerance				12	dB

5.4. Receiver Optical Characteristic

Table.4 Receiver Optical Characteristic

Parameter	Symbol	Min	Typ	Max.	Units	Conditions
Center wavelength	λ_r	840	850	860	nm	
Average Receiver Sensitivity(AVG, EOL)					nm	Standard deviation
Stressed Receiver Sensitivity(OMA, EOL)				-5.2	dBm	Each lane
Saturation power (EOL)		2.4			dBm	Each lane
Max Input power		3.4			dB	
LOS Assert	LOS_A	-30			dBm	Each lane
LOS Dessert	LOS_D			-7.5	dBm	Each lane
LOS Hysteresis		0.5			dB	
Receiver Reflectance				-12	dB	
Signaling rate, each lane			25.78		Gbps	

5.5. Electrical Specification

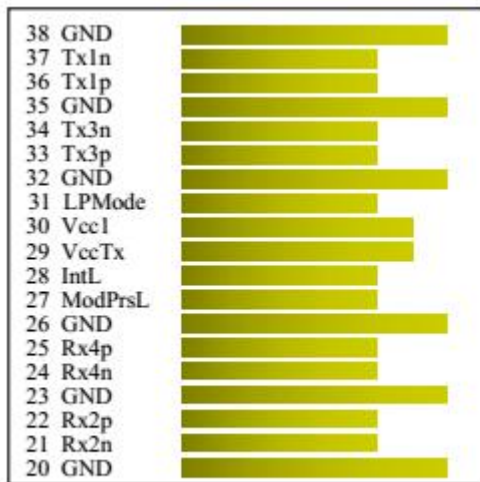
Table.5 Electrical Specification

Parameter	Symbol	Min	Typ	Max.	Units	Conditions
Differential input impedance	Zin	90	100	110	ohm	
Differential output impedance	Zout	90	100	110	ohm	
Differential input voltage amplitude	ΔV_{in}	300		1100	mVp-p	
Differential output voltage amplitude	ΔV_{out}	500		800	mVp-p	
Skew	Sw			300	ps	
Bit Error Rate	BER		E-5			
Input Logic Level High	V _{IH}	2.0		VCC	V	
Input Logic Level Low	V _{IL}	0		0.8	V	
Output Logic Level High	V _{OH}	VCC-0.5		VCC	V	
Output Logic Level Low	V _{OL}	0		0.4	V	

Note:

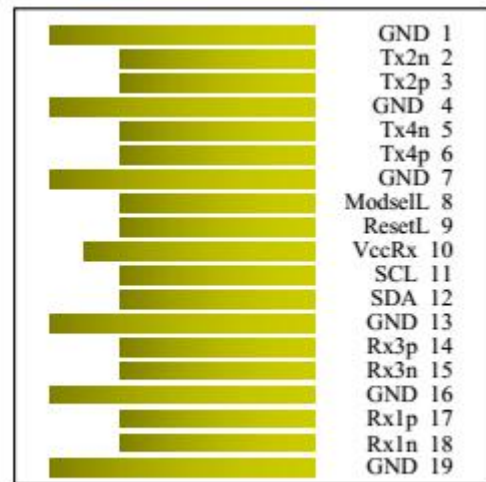
1. BER=10⁻⁵; PRBS 2³¹-1@25.78125Gbps.
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.

5.6. Pin Definitions



Top Side (Viewed From Top)

Module Card Edge



Bottom Side (Viewed From Bottom)

Table.6 Pin Definitions

Pin number	Logic	Symbol	Signal	Description
1		GND	Signal Ground	Ground
2	CML-I	Tx2n	Tx2n	Transmitter Inverted Date Input.AC coupled
3	CML-I	Tx2p	Tx2p	Transmitter Non_Inverted Date Input.AC coupled
4		GND	Signal Ground	Ground
5	CML-I	Tx4n	Tx4n	Transmitter Inverted Date Input.AC coupled
6	CML-I	Tx4p	Tx4p	Transmitter Non_Inverted Date Input.AC coupled
7		GND	Signal Ground	Ground
8	LVTTL-I	ModSell	ModSell	Module Select pin.Selected when held low by the host.
9	LVTTL-I	ResetL	LPMoDe_Reset	Module Reset.A"low" pulse induces a reset on the module.
10		Vcc Rx	Vcc Rx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	SCL	2-wire serial interface
12	LVC MOS-I/O	SDA	SDA	
13		GND	Signal Ground	Ground
14	CML-O	Rx3p	Rx3p	Receiver Non_Inverted Date Input.AC coupled
15	CML-O	Rx3n	Rx3n	Receiver Inverted Date Input.AC coupled
16		GND	Signal Ground	Ground
17	CML-O	Rx1p	Rx1p	Receiver Non_Inverted Date Input.AC coupled
18	CML-O	Rx1n	Rx1n	Receiver Inverted Date Input.AC coupled
19		GND	Signal Ground	Ground
20		GND	Signal Ground	Ground
21	CML-O	Rx2n	Rx2n	Receiver Inverted Date Input.AC coupled
22	CML-O	Rx2p	Rx2p	Receiver Non_Inverted Date Input.AC coupled
23		GND	Signal Ground	Ground
24	CML-O	Rx4n	Rx4n	Receiver Inverted Date Input.AC coupled
25	CML-O	Rx4p	Rx4p	Receiver Non_Inverted Date Input.AC coupled
26		GND	Signal Ground	Ground
27	LVTTL-O	ModPrsL	ModPrsL	Module Present pin.Internally grounded inside the module.
28	LVTTL-O	IntL	IntL	Interrupt by the QSFP module."Low"indicates an Alarm/Warning.
29		Vcc Tx	Vcc Tx	+3.3V Power Supply Transmitter
30		Vccl	Vccl	+3.3V Power Supply
31	LVTTL-I	LPMoDe	LPMoDe	Low Power Mode
32		GND	Signal Ground	Ground
33	CML-I	Tx3p	Tx3p	Transmitter Non_Inverted Date Input.AC coupled
34	CML-I	Tx3n	Tx3n	Transmitter Inverted Date Input.AC coupled
35		GND	Signal Ground	Ground
36	CML-I	Tx1p	Tx1p	Transmitter Non_Inverted Date Input.AC coupled
37	CML-I	Tx1n	Tx1n	Transmitter Inverted Date Input.AC coupled
38		GND	Signal Ground	Ground
Housing			Chassis Ground	

5.7. Power supply filtering

The host board should use the power supply filtering shown in Figure 1

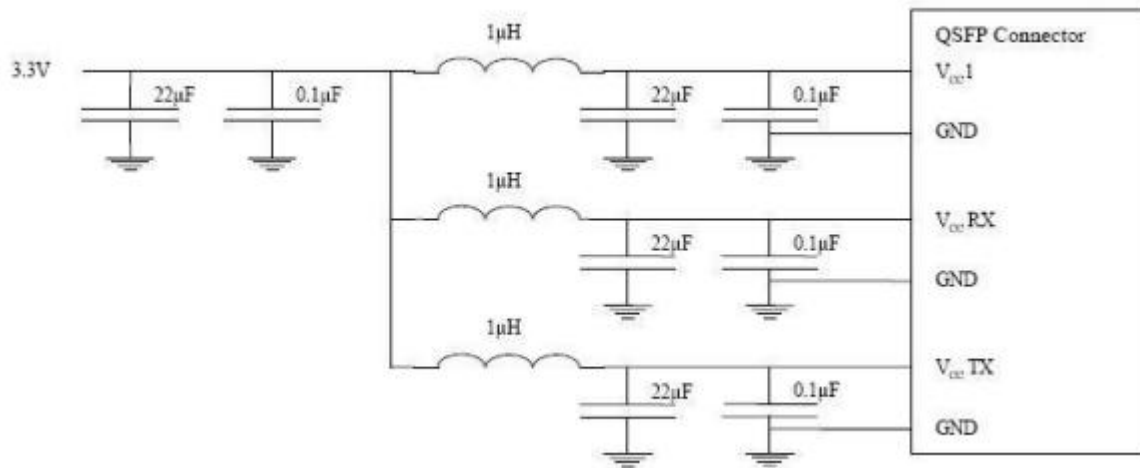


Figure 1:Host Board Power Supply Filtering

5.8 Optical Interface Lanes and Assignment

The optical interface port is a male MPO connector. The four fiber positions on the left as shown in Figure 4, With the key up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1). The central fibers are physically present.

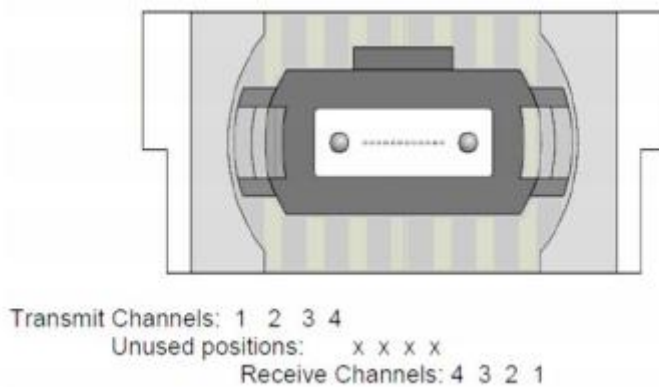


Figure 2:Optical Receptacle and Channel Orientation

5.9. Functional Block Diagram of the QSFP Module

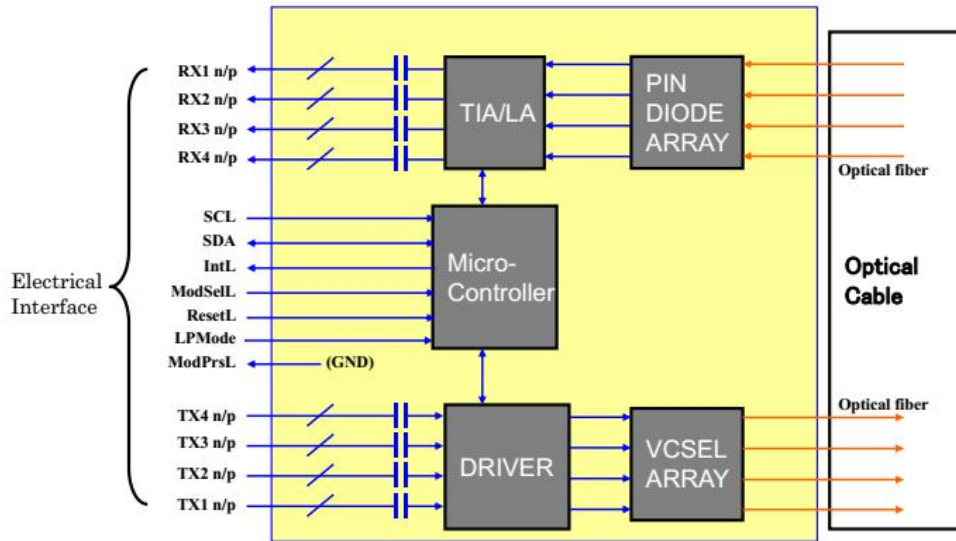


Figure 2:Functional Block Diagram of the QSFP Module

5.10. Mechanical Dimensions

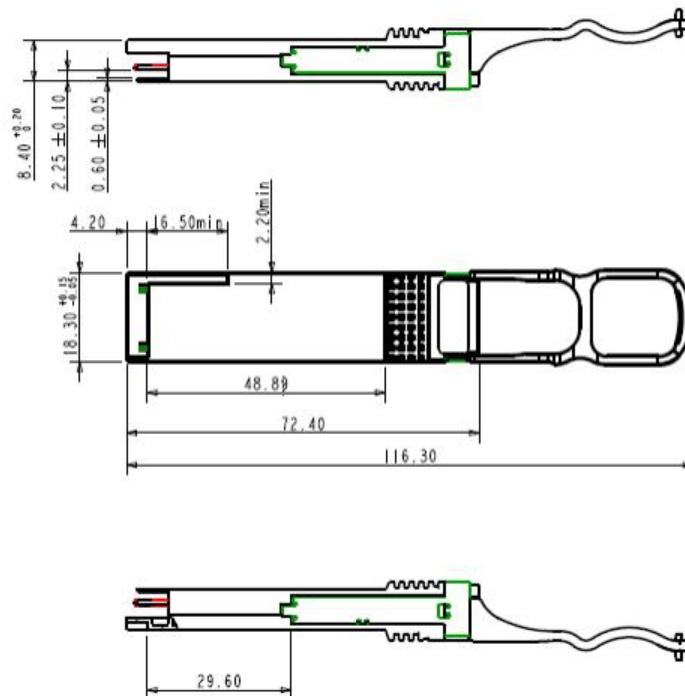


Figure 3:Mechanical Specifications

6. Application Cautions

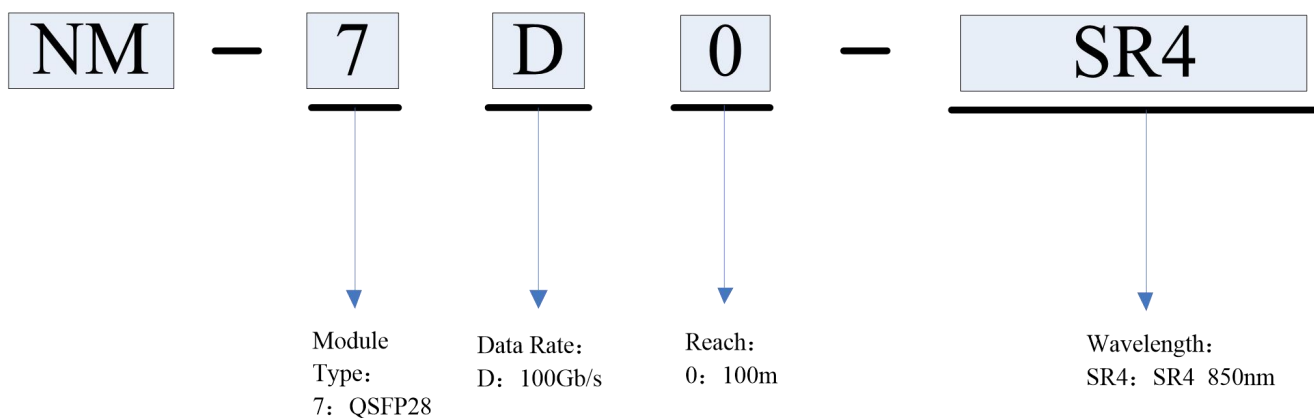
6.1. ESD

This transceiver is specified as ESD threshold 1kV for high speed pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

6.2. LASER SAFTY

This is a Class 1 Laser Product according to IEC 60825-1:1993:+A1:1997+A2:2001. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (July 26, 2001)

7. Order Information



Further Information

For further information, please contact NEME.

Tel: 0086-400-966-4008

Fax: 0086-0755-86152561

Web: www.nemengine.com

Add: 3/F, 20th Bldg. Guangqian Ind Zone. No.3 Longzhu Rd. Nanshan Dist. S.Z City, CHINA.

Shenzhen NEM Engine Technology Co., Ltd.

Tel: 0086-400-966-4008

Fax: 0086-0755-86152561

E-mail: info@nemengine.com

Web: www.nemengine.com