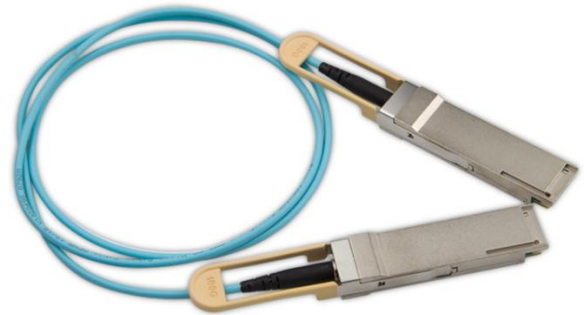


# 100Gbps QSFP28 Active Optical Cable

## NA-A7DMX-XXX

### 1. Applications

- Low-latency and high-speed interconnections for high performance computing(HPC)
- 100G Ethernet
- Other high-throughput data transmission network



### 2. Features

- Quad Small Form-factor Pluggable (QSFP)
- Maximum Aggregate Data Rate 100Gbps
- EDR, FDR, QDR, DDR, SDR (Infiniband)
- 10/25/40/100G Ethernet
- Bi-directional parallel link
- BER<1e-12 From 0 to 50 degree case temp
- CDR no/off automatically
- 10/14/25/28Gb/s per lane, x4 channels
- Up to 70m (OM3)
- Up to 100m (OM4)
- Low power consumption
- Round multi-mode fiber array
- 850nm VCSEL four array
- PIN diode four array

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- Hot-Pluggable
- I2C management interface
- 3.3V power supply voltage
- Maximum 2W power consumption

### **3. Description**

NEM Engine's NA-A7DM3-XXX series are active optical cables (AOC) that allows bi-directional 100Gbps transmission suitable for high performance computing (HPC) clustering and other high-throughput data network, with advantages such as high speed, high density, low latency, low power consumption and light weight.

### **4. standard**

- Compliant with IEEE 802.3bm 100GBASE SR4
- Compliant with InfiniBand EDR,FDR,QDR,DDR,SDR
- Compliant with QSFP MSA(SFF-8665,SFF-8661)
- Compliant with QSFP Common Management SFF-8636
- RoHS Compliant:lead-free

## **4. Performance Specifications**

### **4.1. Absolute Maximum Ratings**

These values represent the damage threshold of the module. Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions.

**Table.1 Absolute maximum ratings**

Parameter	Conditions	Min	Max	Units
Power supply voltage at 3.3V		-0.5	3.75	V
Voltage on I/O pads		-0.5	VDD+0.5	V
Differential Input Swing			1.5	Vpp
Storage temperature	Non-condensing	-40	85	Celsius
Powered case temperature range	Non-condensing	-5	70	Celsius
Relative Humidity		5	85	%
Static discharge voltage on high speed pins	Human body model		500	V
Static discharge voltage on other pins	Human body model		2000	V
Air discharge to QSFP case	EN61000-4-2 Criterion B Test		15	kV
Contact discharge to QSFP case	EN61000-4-2 Criterion B Test		8	kV

## 4.2. Recommended Operating Conditions

**Table.2 Recommended Operating Conditions**

Parameter	Conditions	Min	Typ.	Max	Units
Data rate per lane	8B/10B Coding, 64B/66B Coding	1		26	Gbps
3.3V Supply Voltage		3.13	3.3	3.47	V
Power supply noise including ripples	1kHz to frequency of operation measured at VCC_HOST			50	mVpp
Case temperature		0	35	70	Celsius

## 4.3. Transmitter Specification (Electrical)

**Table.3 Transmitter Specification (Electrical)**

Symbol	Parameter	Specification value.	Unit	Note
X1,X2	Eye mask parameter,time	0.11,0.31	UI	At FDR,EDR rates See Figure 1
Y1,Y2	Eye mask parameter,voltage	95,350	mV	
X	Eye mask parameter,time	0.15	UI	At SDR,DDR rates See Figure 2
Y1,Y2	Eye mask parameter,voltage	250,600	mV	

Symbol	Parameter	Min	Typical	Max.	Unit	Notes
<b>DDPWS</b>	Data Dependent pulse Width Shrinkage			0.11	UI	
<b>J2</b>	J2 jitter tolerance			0.19	UI	With TX CDR bypassed (i.e., disabled)
				0.44	UI	With TX CDR enabled
<b>J9</b>	J9 jitter tolerance			0.34	UI	With TX CDR bypassed (i.e., disabled)
				0.69	UI	With TX CDR enabled
<b>S<sub>DD11</sub></b>	Differential input return loss				dB	See Equation 1 & Figure 3
<b>S<sub>CC11</sub></b>	Common mode input return loss			-2	dB	
<b>S<sub>DC11</sub></b>	Common mode to differential reflection				dB	See Equation 2 & Figure 4
	Skew between channels			50	ps	Skew resulted from module.

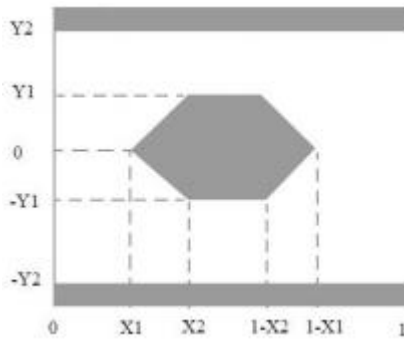


Figure 1

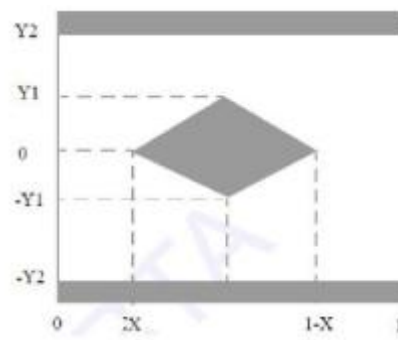


Figure 2

#### 4.4. Receiver Specification(Electrical)

*Table.4 Receiver Specification (Electrical)*

Symbol	Parameter	Specification value.	Unit	Notes
<b>X</b>	Eye mask parameter,time	0.3	UI	Hit ratio=5E-5
<b>Y1,Y2</b>	Eye mask parameter,voltage range 0 range 1 range 2	50,225 100,350 150,450	mV	

Symbol	Parameter	Min	Typical	Max.	Unit	Notes
	Differential Output swing(p-p)		320 (range 0)		mV	Amplitude code 0000 Amplitude code is set at page03 byte 238-239, 4 bits for each channel. See details in the section “Memory Map”
			420 (range 1)		mV	Factory default Amplitude code 0001
			TBD (range 2)		mV	Amplitude code 0010&0011
				50	mV	Squelched state
<b>SDD22</b>	Differential output return loss				dB	See Equation 1 & Figure 3
<b>SCC22</b>	Common mode output return loss			-2	dB	
<b>SDC22</b>	Common mode to differential reflection				dB	See Equation 2 & Figure 4
<b>J2</b>	J2 jitter			0.44	UI	
<b>J9</b>	J9 jitter			0.69	UI	
	Skew between channels			50	ps	Skew resulted from module.

## 4.5. Data Rate Specification

**Table.5 Data Rate Specification**

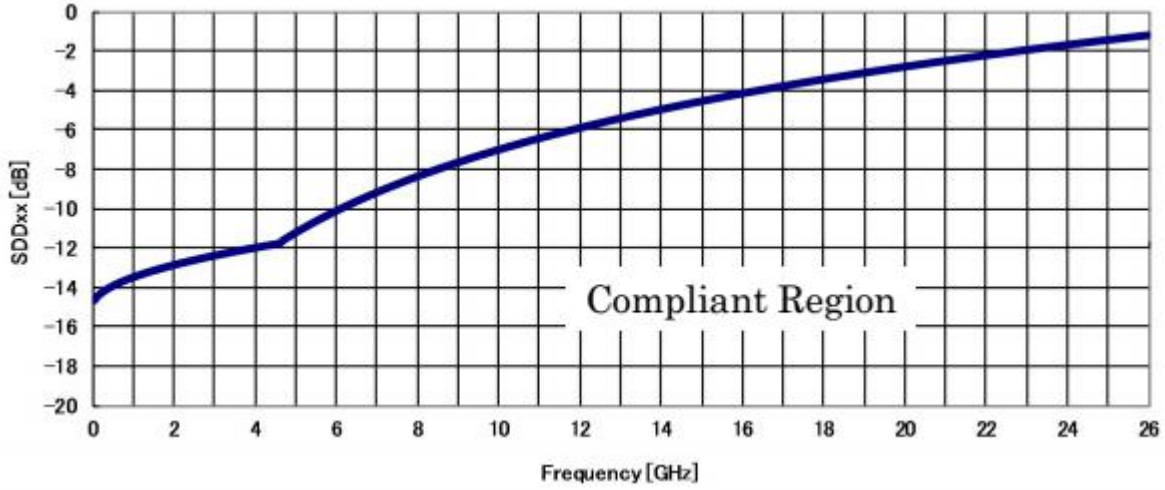
Symbol	Parameter	Min	Typical	Max.	Unit	Notes
<b>BR</b>	Bit Rate per Lane	10	25.781	28	Gbps	Lower BER performance at 28Gbps
<b>BER</b>	Bit Error Rate			$10^{-12}$		1.2.3

1.Bit Error Rate is tested with PRBS 231-1 pattern at 25.781Gbit/s.

2.100G QSFP28 AOC requires an electrical connector compliant with SFF-8662 or SFF-8672 which is used on the host board in order to guarantee its electrical interface specification.

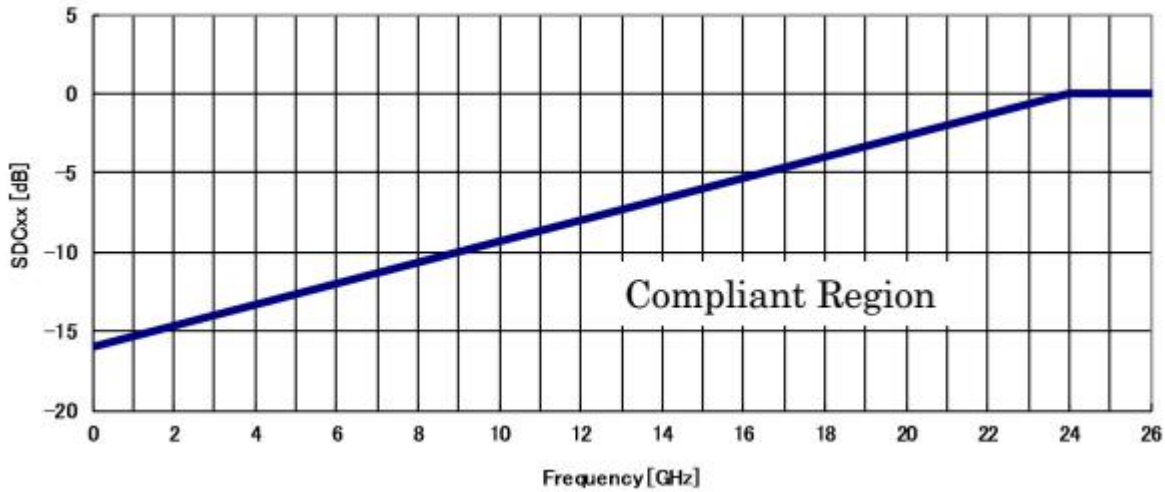
3.Subject to operating condition. Temperature range tested: 25°C ~ < 60°C.

Equation1: 
$$S_{DDxx} \leq \begin{cases} -15 + 1.5\sqrt{f} & 0.05 \leq f < 4.6 \\ -10.66 + 14 * \log_{10}(f / 5.5) & 4.6 \leq f < 26 \end{cases} \quad f \text{ is frequency in GHz}$$



**Figure 3: Limits on S<sub>DD11</sub> and S<sub>DD22</sub> vs.Frequency for EDR**

Equation2: 
$$S_{DCxx} \leq \text{MIN}(-16 + \frac{2}{3}f, 0) \quad 0.05 \leq f < 26 \quad f \text{ is frequency in GHz}$$



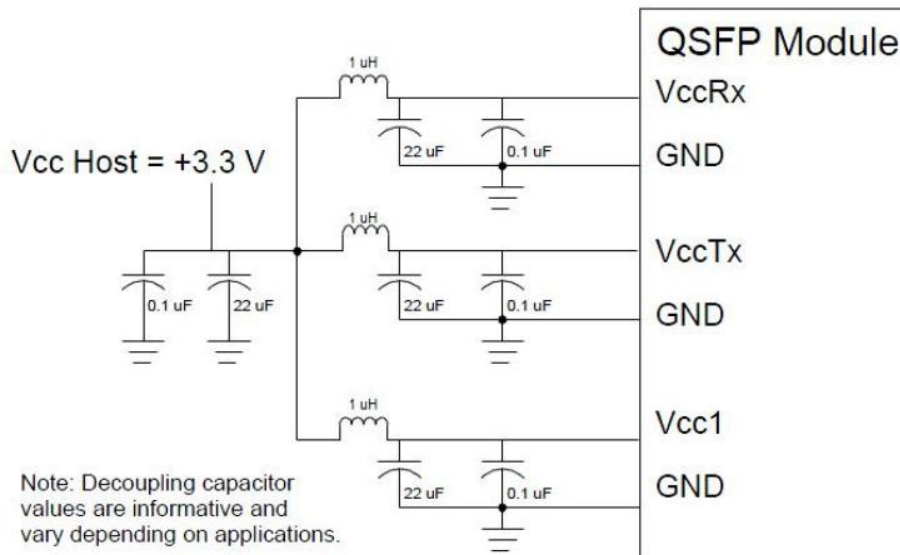
**Figure 4: Limits on S<sub>DC11</sub> and S<sub>DC22</sub> vs.Frequency for EDR**

### 4.6. Low Speed Electrical Specification

*Table.6 Low Speed Electrical Specification*

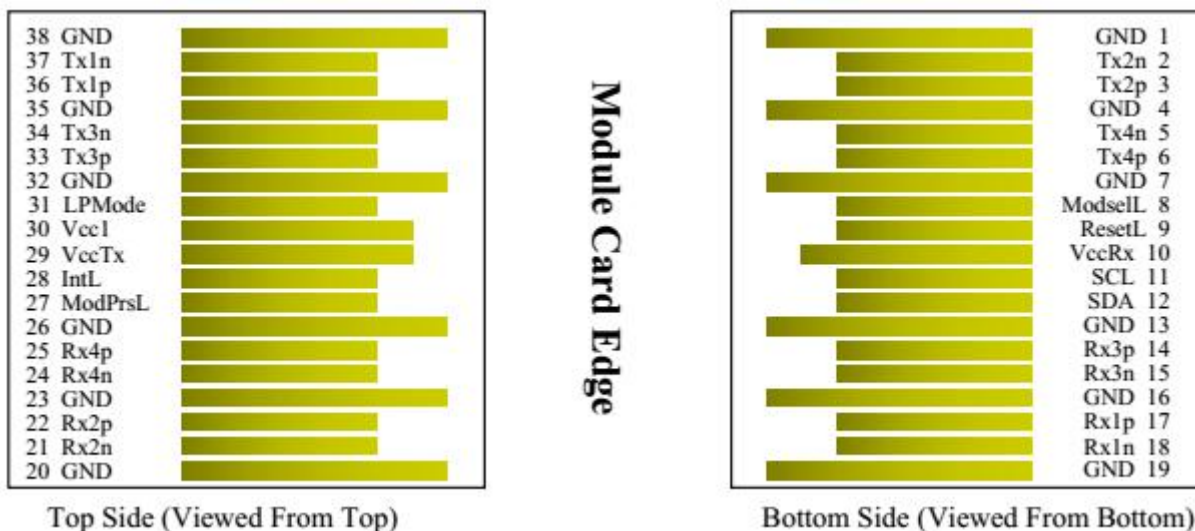
Parameter	Symbol	Min	Max.	Unit	Notes
Reset,ModSell,LPMode	VIL	-0.3	0.8	V	Lower BER performance at 28Gbps
	VIH	2	VCC+0.3	V	
ModPraL					Internally terminated to GND
IntL	VOL	0	0.4	V	IOL=2mA
	VOH	VCC-0.5	VCC+0.3	V	
SCL,SDA	VOL	0	0.4	V	IOL(max)=3mA
	VOH	VCC-0.5	VCC+0.3	V	
	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
Capacitance for SCL and SDA I/O Pin	Ci		14	pF	
Total bus capacitice load for SCL and SDA	Cb		100	pF	3.0kohm Pullup resistor,max
			200	pF	1.6kohm Pullup resistor,max

### 4.7. Recommended QSFP Host Board Power Supply Filtering



**Figure 5: Recommended QSFP Host Board Power Supply Filtering**

**4.8. Pin Definitions**



Top Side (Viewed From Top)

Bottom Side (Viewed From Bottom)

**Table.7 Pin Definitions**

Pin number	Logic	Symbol	Signal	Description
1		GND	Signal Ground	Ground
2	CML-I	Tx2n	Tx2n	Transmitter Inverted Date Input.AC coupled
3	CML-I	Tx2p	Tx2p	Transmitter Non_Inverted Date Input.AC coupled
4		GND	Signal Ground	Ground
5	CML-I	Tx4n	Tx4n	Transmitter Inverted Date Input.AC coupled
6	CML-I	Tx4p	Tx4p	Transmitter Non_Inverted Date Input.AC coupled
7		GND	Signal Ground	Ground
8	LVTTL-I	ModSell	ModSell	Module Select pin.Selected when held low by the host.
9	LVTTL-I	ResetL	LPMoDe_ReseT	Module Reset.A"low" pulse induces a reset on the module.
10		Vcc Rx	Vcc Rx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	SCL	2-wire serial interface
12	LVC MOS-I/O	SDA	SDA	
13		GND	Signal Ground	Ground
14	CML-O	Rx3p	Rx3p	Receiver Non_Inverted Date Input.AC coupled
15	CML-O	Rx3n	Rx3n	Receiver Inverted Date Input.AC coupled
16		GND	Signal Ground	Ground
17	CML-O	Rx1p	Rx1p	Receiver Non_Inverted Date Input.AC coupled
18	CML-O	Rx1n	Rx1n	Receiver Inverted Date Input.AC coupled
19		GND	Signal Ground	Ground
20		GND	Signal Ground	Ground
21	CML-O	Rx2n	Rx2n	Receiver Inverted Date Input.AC coupled
22	CML-O	Rx2p	Rx2p	Receiver Non_Inverted Date Input.AC coupled
23		GND	Signal Ground	Ground
24	CML-O	Rx4n	Rx4n	Receiver Inverted Date Input.AC coupled
25	CML-O	Rx4p	Rx4p	Receiver Non_Inverted Date Input.AC coupled
26		GND	Signal Ground	Ground
27	LVTTL-O	ModPrsL	ModPrsL	Module Present pin.Internally grounded inside the module.
28	LVTTL-O	IntL	IntL	Interrupt by the QSFP module."Low"indicates an Alarm/Warning.
29		Vcc Tx	Vcc Tx	+3.3V Power Supply Transmitter



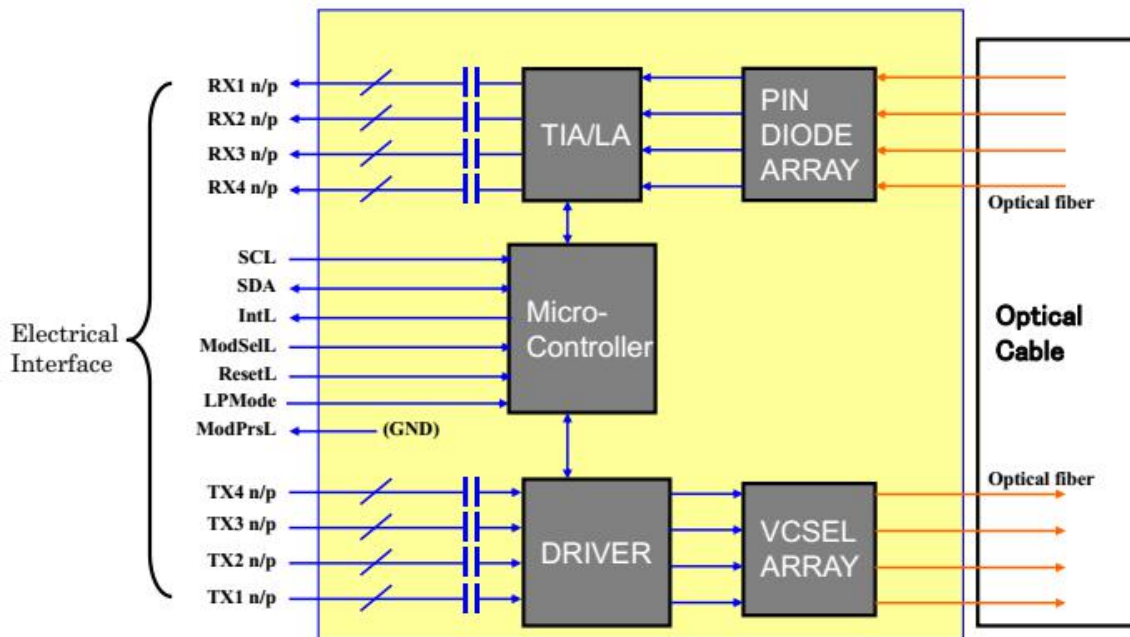
30		Vccl	Vccl	+3.3V Power Supply
31	LVTTL-I	LPMode	LPMode	Low Power Mode
32		GND	Signal Ground	Ground
33	CML-I	Tx3p	Tx3p	Transmitter Non_Inverted Date Input.AC coupled
34	CML-I	Tx3n	Tx3n	Transmitter Inverted Date Input.AC coupled
35		GND	Signal Ground	Ground
36	CML-I	Tx1p	Tx1p	Transmitter Non_Inverted Date Input.AC coupled
37	CML-I	Tx1n	Tx1n	Transmitter Inverted Date Input.AC coupled
38		GND	Signal Ground	Ground
Housing			Chassis Ground	

**4.9. Mechanical Specifications**

*Table.8 Mechanical Specifications*

Parameter	Min	Max.	Unit	Notes
Optical fiber bend radius	30		mm	
QSFP module insertion		40	N	
QSFP module extraction		30	N	
Retention Load	100		N	No damage to module below 100N
Insertion/removal cycles	200		Cycles	Number of cycles for an individual module

**4.10. Functional Block Diagram of the QSFP Module**



**Figure 6:Functional Block Diagram of the QSFP Module**

#### 4.11. Overview of Cable Assembly

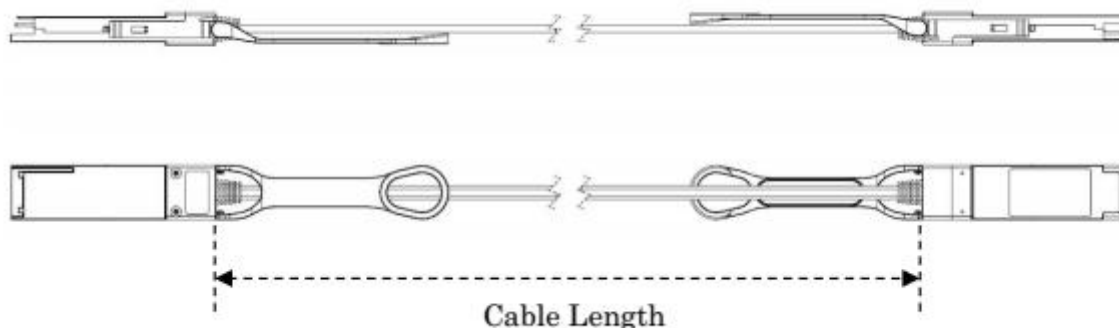


Figure 7: Overview of Cable Assembly

### 5. Application Cautions

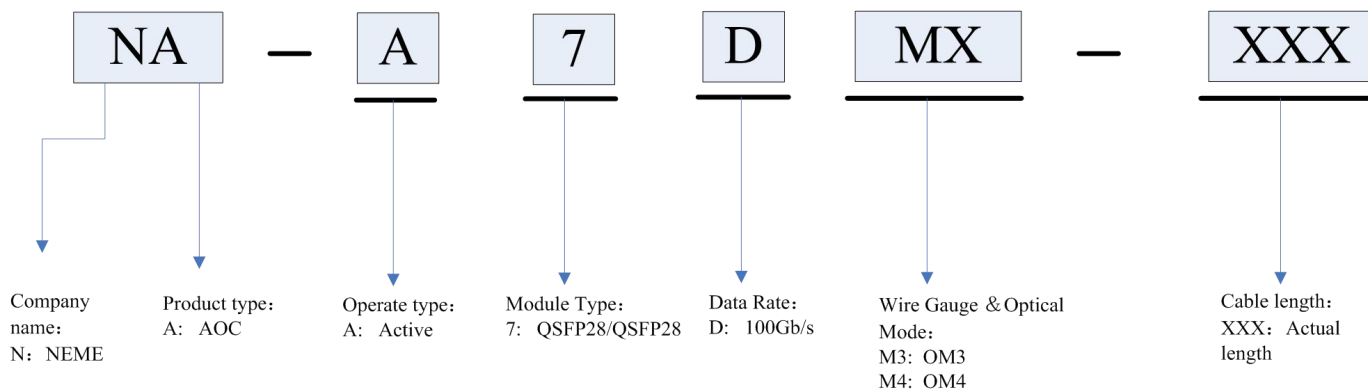
#### 5.1. ESD

This transceiver is specified as ESD threshold 1kV for high speed pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

#### 5.2. LASER SAFTY

This is a Class 1 Laser Product according to IEC 60825-1:1993:+A1:1997+A2:2001. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (July 26, 2001)

## 6. Order Information



## Further Information

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