

# 40Gbps QSFP+ Active Optical Cable

## 1. Applications

- Low-latency and high-speed interconnections for high performance computing(HPC)
- 40G Ethernet SR4
- Other high-throughput data transmission network
- Storage area Network(SAN)



## 2. Features

- Quad Small Form-factor Pluggable (QSFP)
- 40GBASE-SR4 compliant
- QDR, DDR, SDR (Infiniband) compliant
- Bi-directional parallel link
- 10.3125Gb/s per lane, x4 channels
- Low power consumption
- Bundle multi-mode fiber array
- 850nm VCSEL four array
- PIN diode four array
- Hot-Pluggable
- I2C management interface
- From 0 to 70 degree case temperature
- 3.3V power supply voltage
- Electrical 38-pin connector

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### 3. Description

This series are active optical cables (AOC) that allows bi-directional 40Gbps transmission suitable for Ethernet 40GBASE-SR4 and InfiniBand QDR application and other high-throughput data network, with advantages such as high speed, high density, low latency, low power consumption and light weight.

### 4. Standard

- Compliant with IEEE 802.3ba-2010,Annex 86A for 40GBASE-SR4
- Compliant with InfiniBand QDR,DDR,SDR
- Compliant with QSFP MSA(SFF-8436)
- ROHS Compliant: lead-free

### 5. Performance Specifications

#### 5.1. Absolute Maximum Ratings

These values represent the damage threshold of the module. Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions.

*Table.1 Absolute maximum ratings*

Parameter	Conditions	Min	Max	Units
Power supply voltage at 3.3V		-0.5	3.75	V
Voltage on I/O pads		-0.5	VDD+0.5	V
Differential Input Swing			1.5	Vpp
Storage temperature	Non-condensing	-40	85	Celsius
Powered case temperature range	Non-condensing	-5	70	Celsius
Relative Humidity		5	85	%
Static discharge voltage on high speed pins	Human body model		500	V

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Static discharge voltage on other pins	Human body model		2000	V
Air discharge to QSFP case	EN61000-4-2 Criterion B Test		15	kV
Contact discharge to QSFP case	EN61000-4-2 Criterion B Test		8	kV

### 5.2. Recommended Operating Conditions

*Table.2 Recommended Operating Conditions*

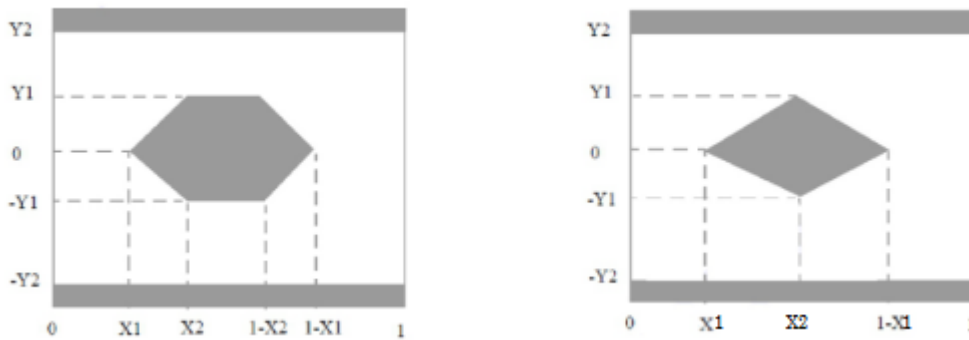
Parameter	Conditions	Min	Typ.	Max	Units
Data rate per lane	8B/10BCoding, 64B/66B Coding	1	10.3125	10.5	Gbps
3.3V Supply Voltage		3.13	3.3	3.47	V
Power supply noise including ripples	1kHz to frequency of operation mersured at VCC_HOST			50	mVpp
Case temperature		0	35	70	Celsius

### 5.3. Transmitter Specification (Electrical)

*Table.3 Transmitter Specification (Electrical)*

Parameter	Test Point	Min	Max.	Units	Conditions
Single ended input voltage tolerance	TP1a	-0.3	4	V	Referred to TP1 signal common(Internally AC coupled)
Differential input voltage swing	TP1a	200	1600	mVpp	Peak to peak differential
AC common-mode input voltage tolerance	TP1a	15	-	mV	RMS
Differential input return loss	TP1	See IEEE 802.3ba 86A.4.1.1	-	dB	10MHz to 11.1GHz
Differential to common-mode input return loss	TP1	10	-	dB	10MHz to 11.1GHz
J2 jitter tolerance	TP1a	0.17	-	UI	
J9 jitter tolerance	TP1a	0.29	-	UI	
Data Dependent Pulse Width	TP1a	0.07	-	UI	

Shrinkage (DDPWS) tolerance					
Eye mask coordinates: X1, X2 Y1, Y2	TP1a	Specification values 0.11, 0.31 95, 350		UI mV	Hit ratio = $5 \times 10^{-5}$ see Figure. 3(a)



a) Transmitter electrical input eye mask (b) Receiver electrical output eye mask

Figure 1. Eye Mask

### 5.4. Receiver Specification (Electrical)

Table.4 Receiver Specification (Electrical)

Parameter	Test Point	Min	Typ	Max.	Units	Conditions	
Single ended input voltage tolerance	TP4	-0.3	-	4	V	Referred to signal common (Internally AC coupled)	
AC common-mode input voltage	TP4	-	-	7.5	mV	RMS	
Differential Output swing (p-p)	TP4	-	320 (range 0)	-	mV	See details in the section "Memory Map", page 03, byte 238-239.	
		-	420 (range 1)	-	mV		Default setting
		-	740 (range 2)	-	mV		
		-	-	50	mV	Squelched state	
Termination mismatch at 1MHz	TP4	-	-	5	%		
Differential output return loss	TP4	See IEEE 802.3ba 86A.4.2.1		-	dB	10MHz to 11.1GHz	
Common-mode output return Loss	TP4	See IEEE 802.3ba 86A.4.2.2		-	dB	10MHz to 11.1GHz	

Output transition time, 20% to 80%	TP4	28	-	-	ps	
J2 jitter output	TP4	-	-	0.42	UI	
J9 jitter output	TP4	-	-	0.65	UI	
Eye mask coordinates: X1, X2 Y1, Y2	TP4	Specification values 0.29, 0.5 150, 425			UI mV	Hit ratio = $5 \times 10^{-5}$ see Figure. 3(b)

### 5.5. Test Point Definition

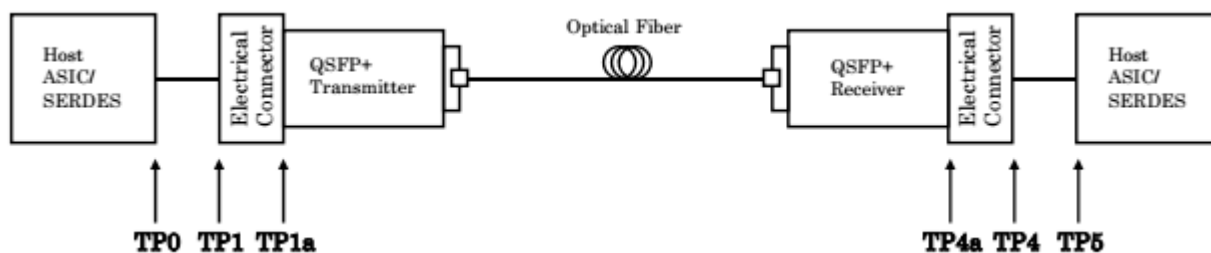


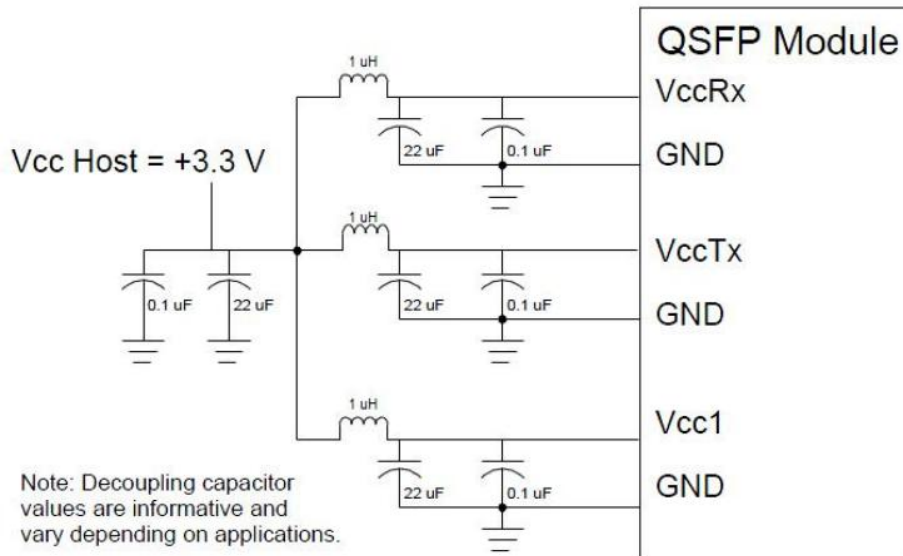
Figure 2. Test Point

### 5.6. Low Speed Electrical Specification

Table.5 Low Speed Electrical Specification

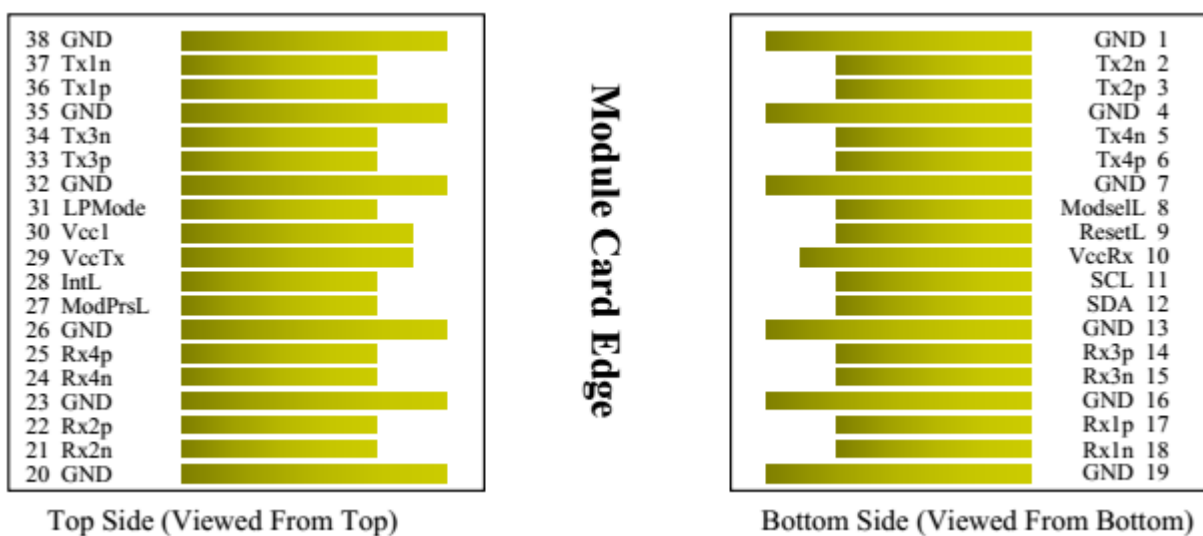
Parameter	Symbol	Min	Max.	Unit	Notes
Reset, ModSell, LPMode	VIL	-0.3	0.8	V	Lower BER performance at 28Gbps
	VIH	2	VCC+0.3	V	
ModPraL					Internally terminated to GND
IntL	VOL	0	0.4	V	IOL=2mA
	VOH	VCC-0.5	VCC+0.3	V	
SCL,SDA	VOL	0	0.4	V	IOL(max)=3mA
	VOH	VCC-0.5	VCC+0.3	V	
	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
Capacitance for SCL and SDA I/O Pin	Ci		14	pF	
Total bus capacitance load for SCL and SDA	Cb		100	pF	3.0kohm Pullup resistor,max
			200	pF	1.6kohm Pullup resistor,max

### 5.7. Recommended QSFP Host Board Power Supply Filtering



**Figure 3: Recommended QSFP Host Board Power Supply Filtering**

### 5.8. Pin Definitions



**Table.6Pin Definitions**

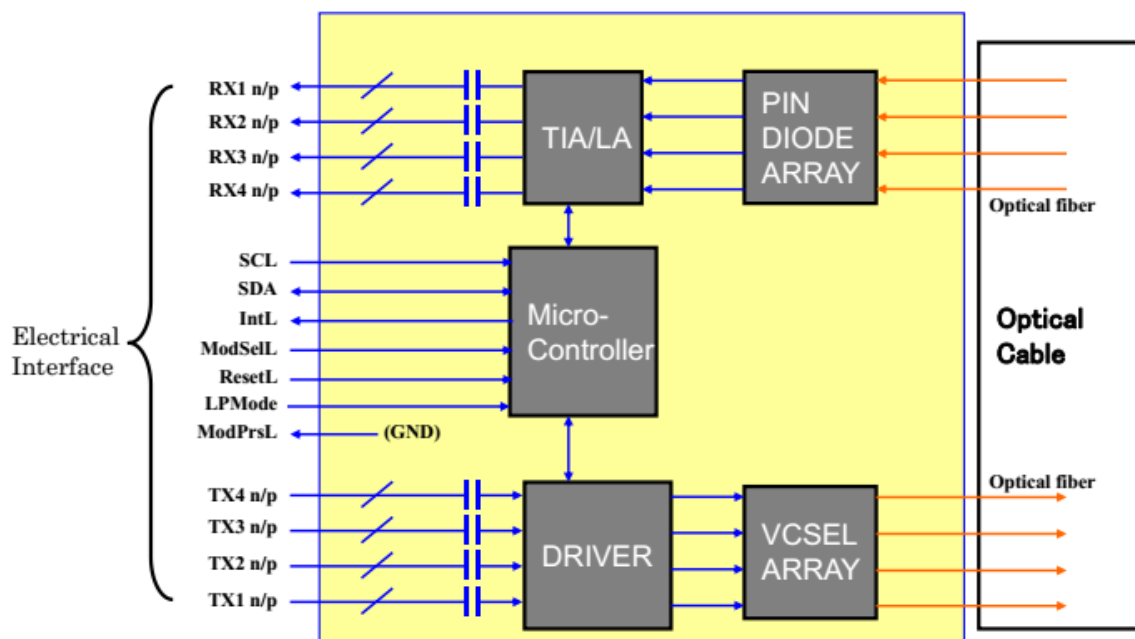
Pin number	Logic	Symbol	Signal	Description
1		GND	Signal Ground	Ground
2	CML-I	Tx2n	Tx2n	Transmitter Inverted Date Input.AC coupled
3	CML-I	Tx2p	Tx2p	Transmitter Non_Inverted Date Input.AC coupled
4		GND	Signal Ground	Ground
5	CML-I	Tx4n	Tx4n	Transmitter Inverted Date Input.AC coupled
6	CML-I	Tx4p	Tx4p	Transmitter Non_Inverted Date Input.AC coupled
7		GND	Signal Ground	Ground
8	LVTTTL-I	ModSelL	ModSelL	Module Select pin.Selected when held low by the host.
9	LVTTTL-I	ResetL	LPMMode_Reset	Module Reset.A"low" pulse induces a reset on the module.
10		Vcc Rx	Vcc Rx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	SCL	2-wire serial interface
12	LVC MOS-I/O	SDA	SDA	
13		GND	Signal Ground	Ground
14	CML-O	Rx3p	Rx3p	Receiver Non_Inverted Date Input.AC coupled
15	CML-O	Rx3n	Rx3n	Receiver Inverted Date Input.AC coupled
16		GND	Signal Ground	Ground
17	CML-O	Rx1p	Rx1p	Receiver Non_Inverted Date Input.AC coupled
18	CML-O	Rx1n	Rx1n	Receiver Inverted Date Input.AC coupled
19		GND	Signal Ground	Ground
20		GND	Signal Ground	Ground
21	CML-O	Rx2n	Rx2n	Receiver Inverted Date Input.AC coupled
22	CML-O	Rx2p	Rx2p	Receiver Non_Inverted Date Input.AC coupled
23		GND	Signal Ground	Ground
24	CML-O	Rx4n	Rx4n	Receiver Inverted Date Input.AC coupled
25	CML-O	Rx4p	Rx4p	Receiver Non_Inverted Date Input.AC coupled
26		GND	Signal Ground	Ground
27	LVTTTL-O	ModPrsL	ModPrsL	Module Present pin.Internally grounded inside the module.
28	LVTTTL-O	IntL	IntL	Interrupt by the QSFP module."Low"indicates an Alarm/Warning.
29		Vcc Tx	Vcc Tx	+3.3V Power Supply Transmitter
30		Vccl	Vccl	+3.3V Power Supply
31	LVTTTL-I	LPMMode	LPMMode	Low Power Mode
32		GND	Signal Ground	Ground
33	CML-I	Tx3p	Tx3p	Transmitter Non_Inverted Date Input.AC coupled
34	CML-I	Tx3n	Tx3n	Transmitter Inverted Date Input.AC coupled
35		GND	Signal Ground	Ground
36	CML-I	Tx1p	Tx1p	Transmitter Non_Inverted Date Input.AC coupled
37	CML-I	Tx1n	Tx1n	Transmitter Inverted Date Input.AC coupled
38		GND	Signal Ground	Ground
Housing			Chassis Ground	

### 5.9. Mechanical Specifications

*Table.7 Mechanical Specifications*

Parameter	Min	Max.	Unit	Notes
Cable bend radius(Installation)	30		mm	
Cable bend radius(Operating)	60			
QSFP module insertion		40	N	
QSFP module extraction		30	N	
Retention Load	100		N	No damage to module below 100N
Insertion/removal cycles	200		Cycles	Number of cycles for an individual module

### 5.10. Functional Block Diagram of the QSFP Module



**Figure 6: Functional Block Diagram of the QSFP Module**



### 5.11. Overview of Cable Assembly

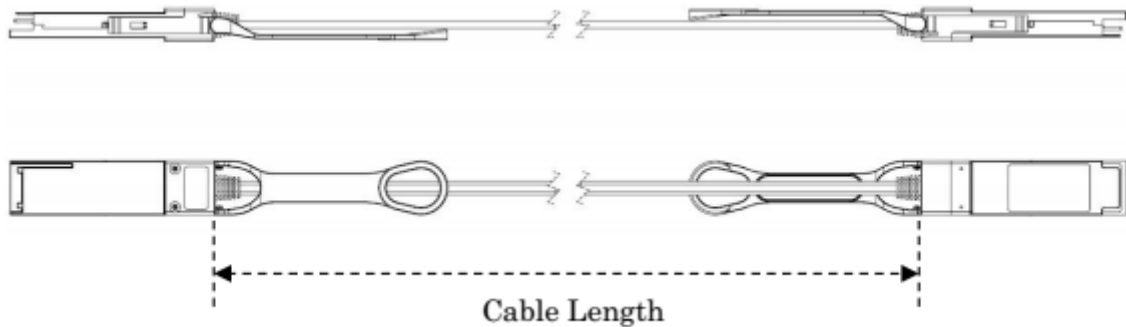


Figure 7: Overview of Cable Assembly

## 6. Application Cautions

### 6.1. ESD

This transceiver is specified as ESD threshold 1kV for high speed pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

### 6.2. LASER SAFETY

This is a Class 1 Laser Product according to IEC 60825-1:1993:+A1:1997+A2:2001. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (July 26, 2001)